

## S72WS-N Based MCP/PoP Products

1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus  
256/512 Mb Simultaneous Read/Write, Burst Mode Flash Memory  
512 Mb NAND Flash  
1024 Mb NAND Interface ORNAND Flash Memory on Bus 1  
512/256/128 Mb (8M/4M/2M x 16-bit x 4 Banks) Mobile SDRAM on  
Bus 2



*Data Sheet (Advance Information)*

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# S72WS-N Based MCP/PoP Products

**1.8 Volt-only x16 Flash Memory and SDRAM on Split Bus**  
**256/512 Mb Simultaneous Read/Write, Burst Mode Flash Memory**  
**512 Mb NAND Flash**  
**1024 Mb NAND Interface ORNAND Flash Memory on Bus 1**  
**512/256/128 Mb (8M/4M/2M x 16-bit x 4 Banks) Mobile SDRAM on Bus 2**



*Data Sheet (Advance Information)*

## Features

- Power supply voltage of 1.7 to 1.95V

### High Performance

- Flash access time: 80 ns for NOR Flash, 25 ns for ORNAND Flash
- Flash burst frequencies: 54 MHz, 66MHz, 80MHz
- Mobile SDRAM burst frequency: 104 MHz, 133 MHz (DDR)

### Package:

- 9.0 x 12.0 mm MCP BGA
- 11.0 x 13.0 mm MCP BGA
- 15.0 x 15.0 x 1.2 mm MCP Package-on-Package (PoP)

### Operating Temperature

- -25°C to +85°C (wireless)

## General Description

The S72WS series is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- One or two NOR flash memory dies
- One NAND Interface ORNAND die
- Separate bus for one or more Mobile SDRAM die

The products covered by this document are listed in the table below.

Device	NOR Flash Density			NAND Flash Density		SDRAM Density		
	512Mb	256Mb	128Mb	1024Mb	512Mb	512Mb	256Mb	128Mb
S72WS256ND0		X						X
S72WS256NDE	X							X
S72WS256NEE	X						X	
S72WS512NFG	X			X		X		
S72WS512NEG	X			X			X	
S72WS512NEF	X				X		X	
S72WS512NFF	X				X	X		

### Note

For a list of PoP OPNs, please contact the local sales representative or refer to the valid combinations tables.

For detailed specifications, please refer to the individual data sheets.

Document	Publication Identification Number (PID)
S29WS256N	S29WS-N_00
S30MS01GP/512P	S30MS-P_00
128 Mb Mobile SDRAM Type 1	SDRAM_01
128 Mb Mobile SDRAM Type 2	SDRAM_05
128 Mb Mobile DDR-DRAM Type 5	SDRAM_07
256 Mb Mobile SDRAM Type 2	SDRAM_05
512 Mb Mobile DDR-DRAM Type 1	SDRAM_09
512 Mb Mobile SDRAM Type 4	SDRAM_06
512 Mb NAND Type 1	NAND_01
512 Mb Mobile DDR-DRAM Type 5	DRAM_04
512 Mb Mobile DDR-DRAM Type 2	DRAM_05

**Publication Number** S72WS-N\_00    **Revision** A    **Amendment** 9    **Issue Date** May 8, 2007

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## 1. Product Selector Guide

### 1.1 NOR Flash + DRAM Products

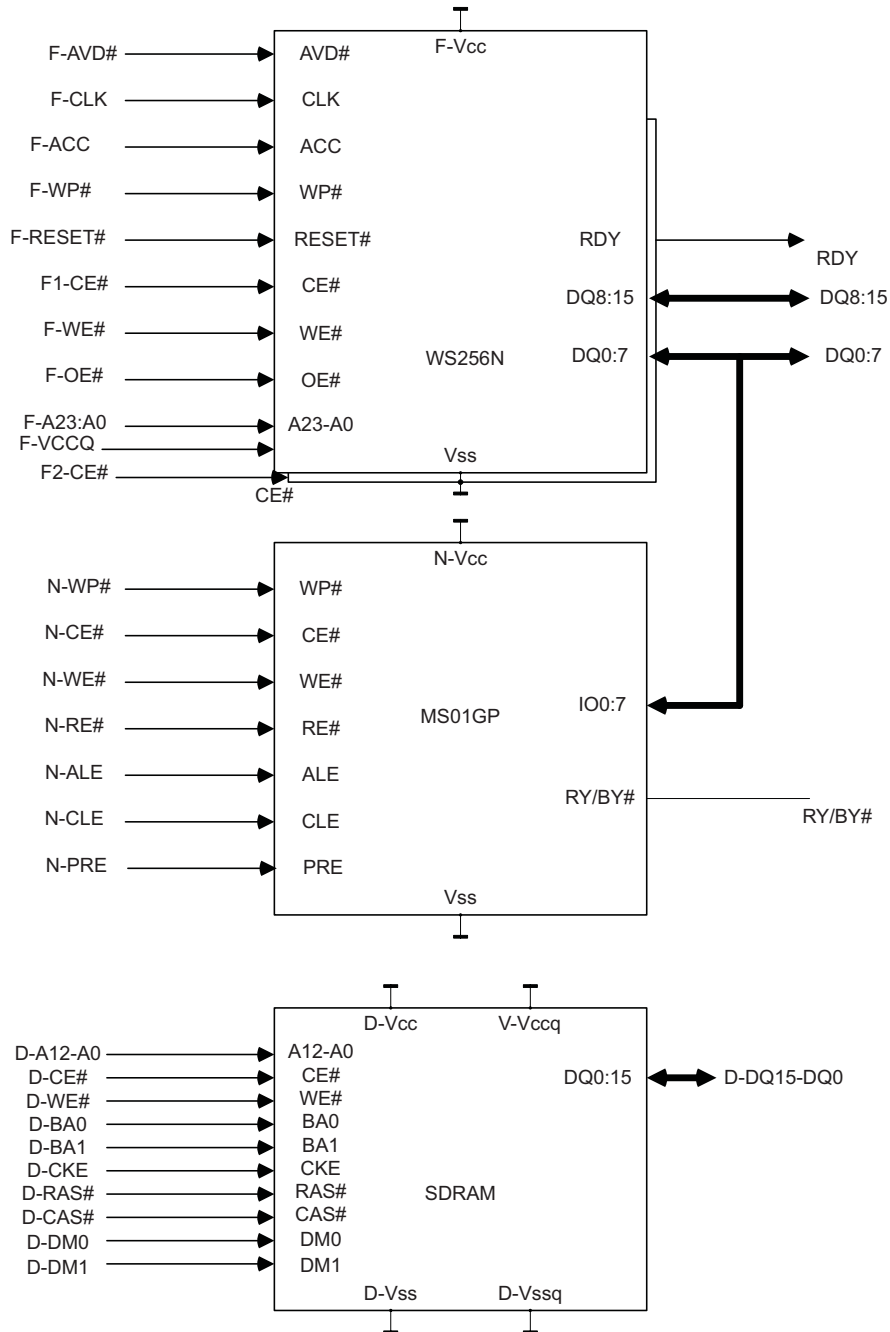
Device-Model#	Flash Density (Code)	Flash Density (Data)	Burst Speed (MHz)	SDRAM Density	SDRAM burst Speed (MHz)	DRAM Supplier	DYB	Package
S72WS256ND0BAWB7	256 Mb	—	54 MHz	128	104 MHz	1	sector unprotected	9x12x1.2
S72WS256ND0BAWB8						2		
S72WS256NDEBAWU7	256 Mb	256 Mb	54 MHz	128	104 MHz	1	sector unprotected	9x12x1.4
S72WS256NDEBAWUB				2				
S72WS256NEEBAWU7				256		1		
S72WS256NEEBAWUB				2				
S72WS256ND0BFWB7	256 Mb	—	54 MHz	128	104 MHz	1	sector unprotected	9x12x1.2
S72WS256ND0BFWB8						2		
S72WS256NDEBFWU7	256 Mb	256 Mb	54 MHz	128	104 MHz	1	sector unprotected	9x12x1.4
S72WS256NDEBFWUB				2				
S72WS256NEEFWU7				256		1		
S72WS256NEEFWUB				2				
S72WS256ND0KFWD3	256 Mb		66 MHz	128	133 MHz (DDR)	5	sector unprotected	15x15x1.25
S72WS256ND0BFW93					133 MHz (DDR)		sector unprotected	9x12x1.2

## 1.2 NOR Flash + ORNAND Flash + DRAM Products

Device-Model#	NOR Flash Density	ORNAND Flash Density	SDRAM Density	Flash Speed	DRAM Speed	Supplier	ORNAND Bus Width	ECC required?	Package
S72WS512NFFBFWZ2	512 Mb	512 Mb (NAND)	512 Mb	66 MHz	133 MHz (DDR)	DRAM Type 1	X16	Yes	11x13x1.4 mm
S72WS512NFFBFWZJ						DRAM Type 5			
S72WS512NFG-L7						DRAM Type 4			
S72WS512NFG-L6		54 MHz							
S72WS512NFG-L5		66 MHz							
S72WS512NFG-47		80 MHz							
S72WS512NFG-46		54 MHz							
S72WS512NFG-46		66 MHz							
S72WS512NFG-45		80 MHz							
S72WS512NFG-LZ		54 MHz							
S72WS512NFG-LY		66 MHz							
S72WS512NFG-LW		80 MHz							
S72WS512NFG-4Z		54 MHz							
S72WS512NFG-4Y		66 MHz							
S72WS512NFG-4W		80 MHz							
S72WS512NFG-N7		DRAM Type 2		X16	No				
S72WS512NFG-N6						54 MHz			
S72WS512NFG-N6						66 MHz			
S72WS512NFG-N5						80 MHz			
S72WS512NFG-67						54 MHz			
S72WS512NFG-66						66 MHz			
S72WS512NFG-65						80 MHz			
S72WS512NFG-NZ						54 MHz			
S72WS512NFG-NY						66 MHz			
S72WS512NFG-NW						80 MHz			
S72WS512NFG-6Z						54 MHz			
S72WS512NFG-6Y						66 MHz			
S72WS512NFG-6W		80 MHz							
S72WS512NEG-LZ		DRAM Type 4		X16	Yes				
S72WS512NEG-LY						54 MHz			
S72WS512NEG-LW						66 MHz			
S72WS512NEG-4Z						80 MHz			
S72WS512NEG-4Y						54 MHz			
S72WS512NEG-4Y	66 MHz								
S72WS512NEG-4W	80 MHz								
S72WS512NEG-NZ	54 MHz								
S72WS512NEG-NY	66 MHz								
S72WS512NEG-NW	80 MHz								
S72WS512NEG-6Z	54 MHz								
S72WS512NEG-6Y	66 MHz								
S72WS512NEG-6W	80 MHz								
S72WS512NEG-LZ	DRAM Type 2	X16	No						
S72WS512NEG-LY				54 MHz					
S72WS512NEG-LW				66 MHz					
S72WS512NEG-4Z				80 MHz					
S72WS512NEG-4Y				54 MHz					
S72WS512NEG-4Y				66 MHz					
S72WS512NEG-4W				80 MHz					
S72WS512NEG-NZ				54 MHz					
S72WS512NEG-NY				66 MHz					
S72WS512NEG-NW				80 MHz					
S72WS512NEG-6Z				54 MHz					
S72WS512NEG-6Y				66 MHz					
S72WS512NEG-6W	80 MHz								
S72WS512NEG-LZ	DRAM Type 2	X16	Yes						
S72WS512NEG-LY				54 MHz					
S72WS512NEG-LW				66 MHz					
S72WS512NEG-4Z				80 MHz					
S72WS512NEG-4Y				54 MHz					
S72WS512NEG-4Y				66 MHz					
S72WS512NEG-4W				80 MHz					
S72WS512NEG-NZ				54 MHz					
S72WS512NEG-NY				66 MHz					
S72WS512NEG-NW				80 MHz					
S72WS512NEG-6Z				54 MHz					
S72WS512NEG-6Y				66 MHz					
S72WS512NEG-6W	80 MHz								
S72WS512NEFKFWHJ	512 Mb	512 Mb (NAND)	256 Mb	66 MHz	133 MHz (DDR)	DRAM Type 2	x16	Yes	15x15x1.25 mm
S72WS512NFFKFWZ2			512 Mb			DRAM Type 1			15x15x1.25 mm
S72WS512NFFKFWZJ			512 Mb			DRAM Type 5			15x15x1.25 mm

## 2. MCP Block Diagram

### 2.1 NOR Flash + ORNAND Flash + DRAM Products



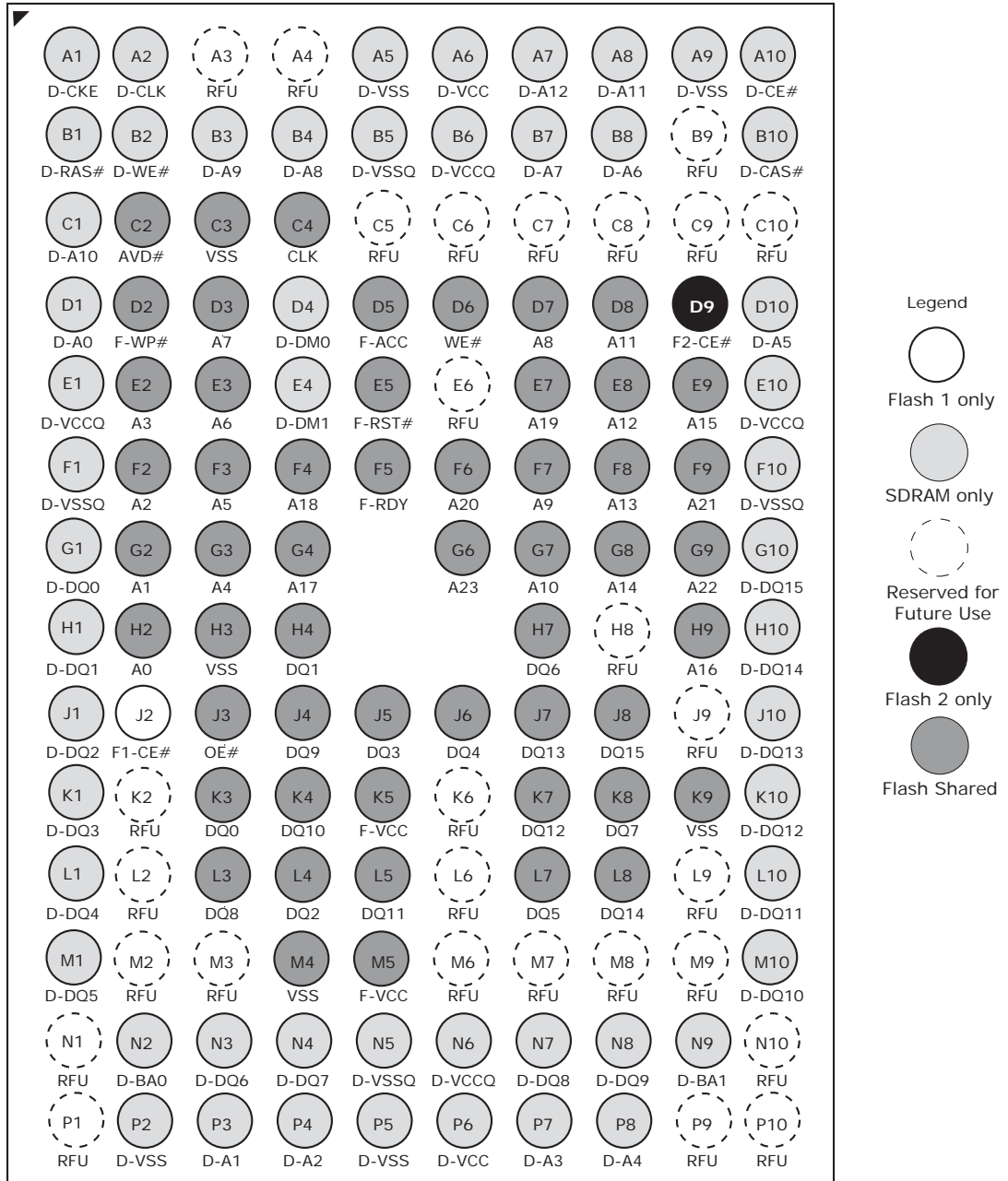
**Notes**

- For a one-Flash configuration, F1-CE# = CE#.  
For a two-Flash configuration, F1-CE# = CE for Flash 1 and F2-CE# = CE for Flash 2; F2-CE# is the chip-enable pin for the second Flash.
- If ORNAND is not present in the MCP, then the MS01GP block will not be present in the figure above. In that case, the common signals go only to the WS256N flash, while the SDRAM signals remain unchanged.
- If ORNAND supports a x16 bus, then NOR DQ0-DQ15 is shared with ORNAND I/O0-I/O15.

### 3. Connection Diagram

#### 3.1 2 x 256Mb NOR Flash with 256Mb SDRAM

137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)

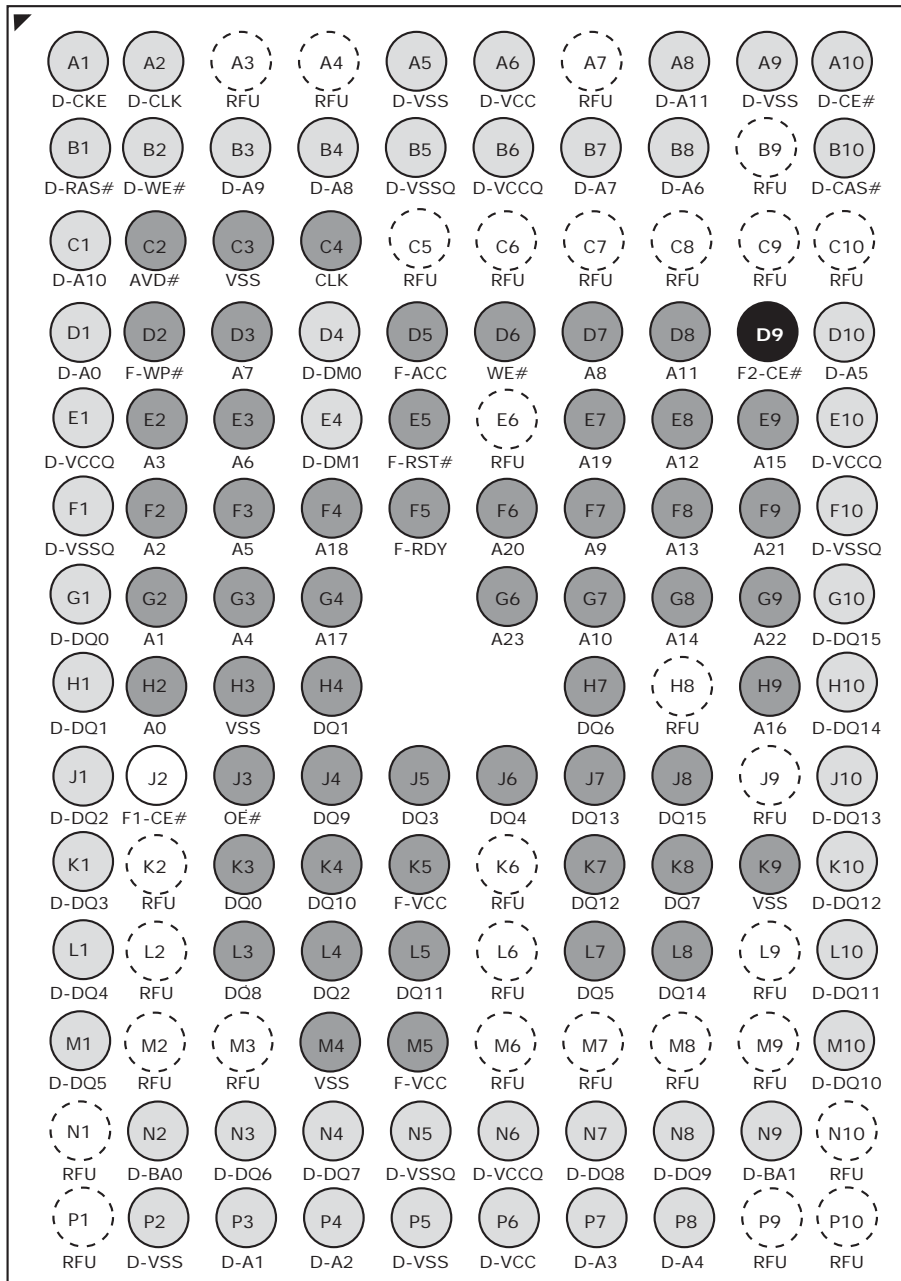


**Note**  
M8 is RFU for SDR-DRAM and F-VCCQ for DDR-DRAM, as indicated in subsequent connection diagrams.



### 3.2 2 x 256Mb NOR Flash with 128Mb SDRAM

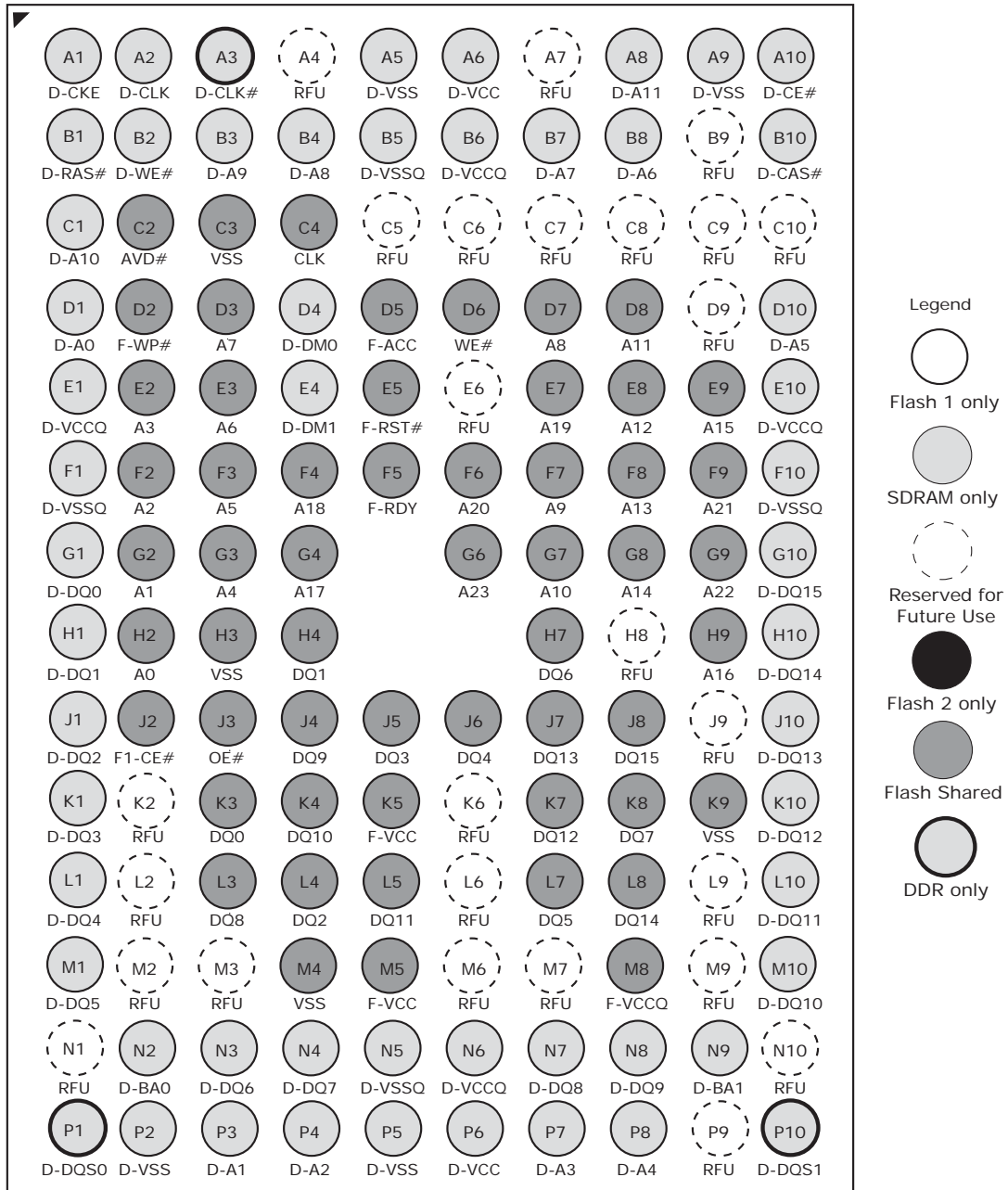
137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)



**Note**  
M8 is RFU for SDR-DRAM and F-VCCQ for DDR-DRAM, as indicated in subsequent connection diagrams.

### 3.3 256Mb NOR Flash with 128Mb SDR/DDR-DRAM

137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)

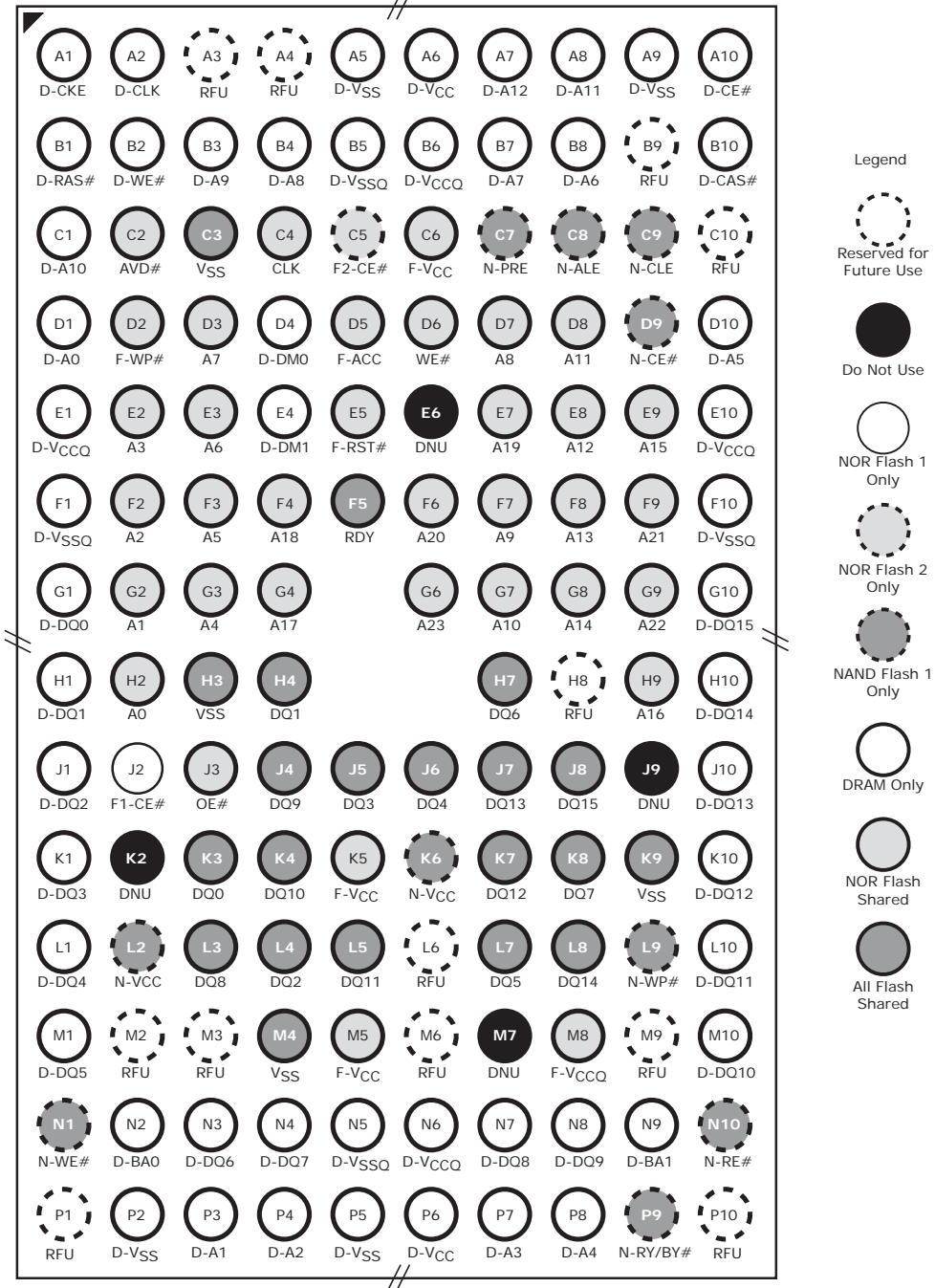


**Note**  
DDR-only signals are RFUs in the case of the SDR-DRAM based MCPs.

### 3.4 512 Mb NOR Flash with 1024-Mb ORNAND on Bus 1 and 512 or 256-Mb SDRAM on Bus 2

#### 3.4.1 x16 ORNAND-based MCP

137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)

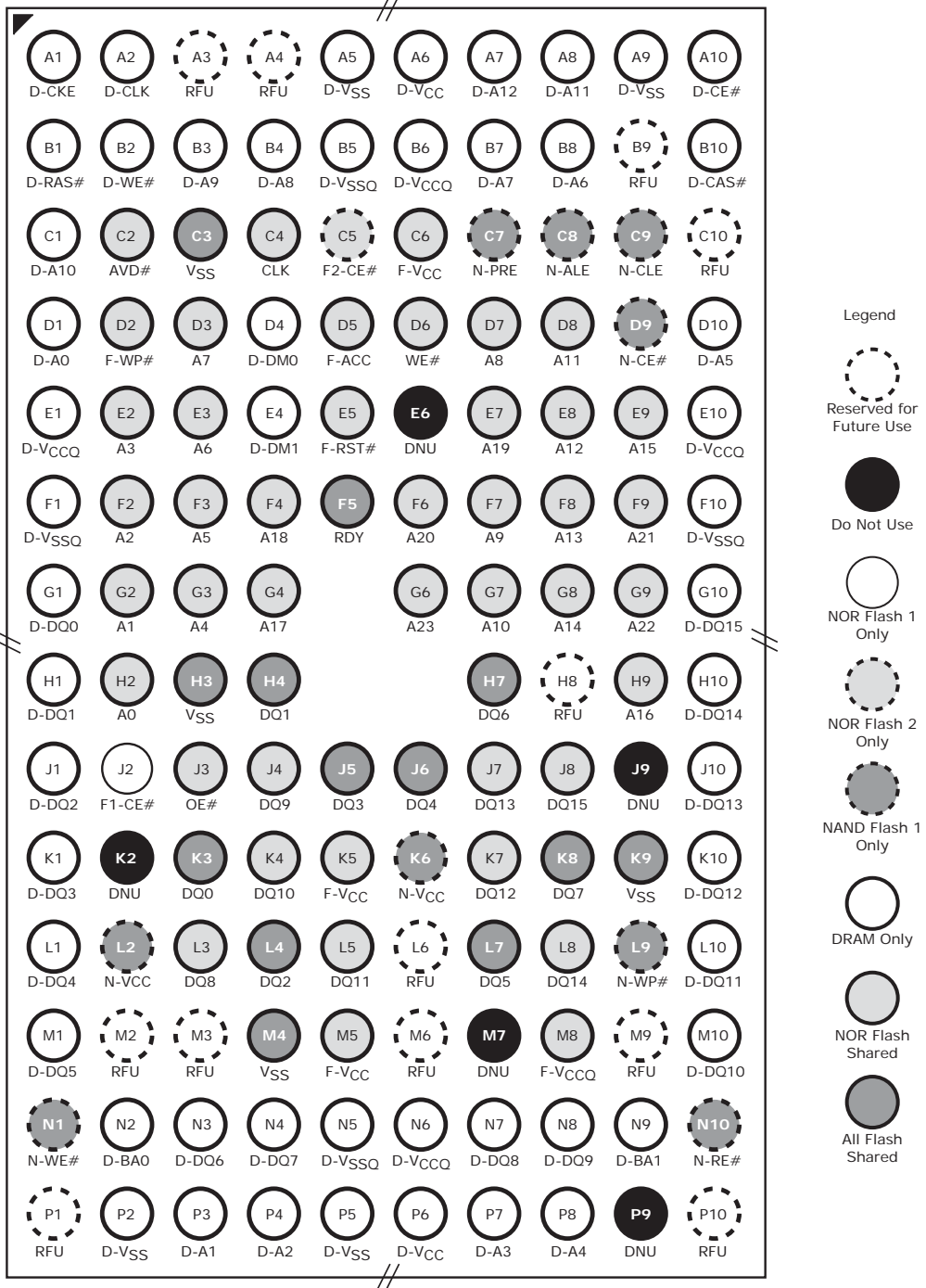


**Note**  
DDR-only signals are RFU in the case of SDR-DRAM based MCPs.

### 3.5 512Mb NOR Flash with 1024-Mb ORNAND on Bus 1 and 512 or 256 Mb SDRAM on Bus 2

#### 3.5.1 x8 ORNAND-based MCP

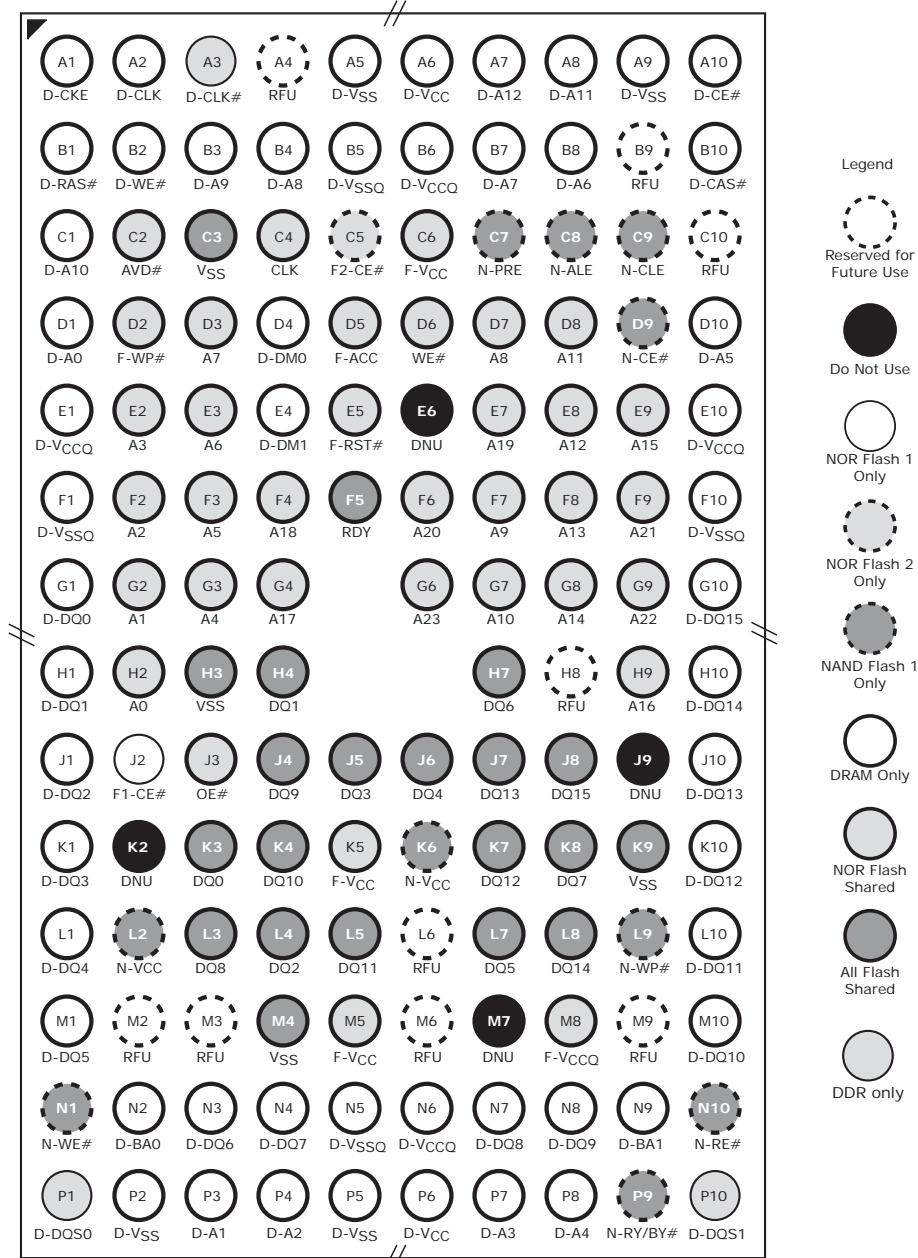
137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)



### 3.6 512Mb NOR Flash with 512-Mb NAND on Bus 1 and 512-Mb SDRAM on Bus 2

#### 3.6.1 x16 ORNAND-based MCP

137-ball Fine-Pitch Ball Grid Array  
(Top View, Balls Facing Down)

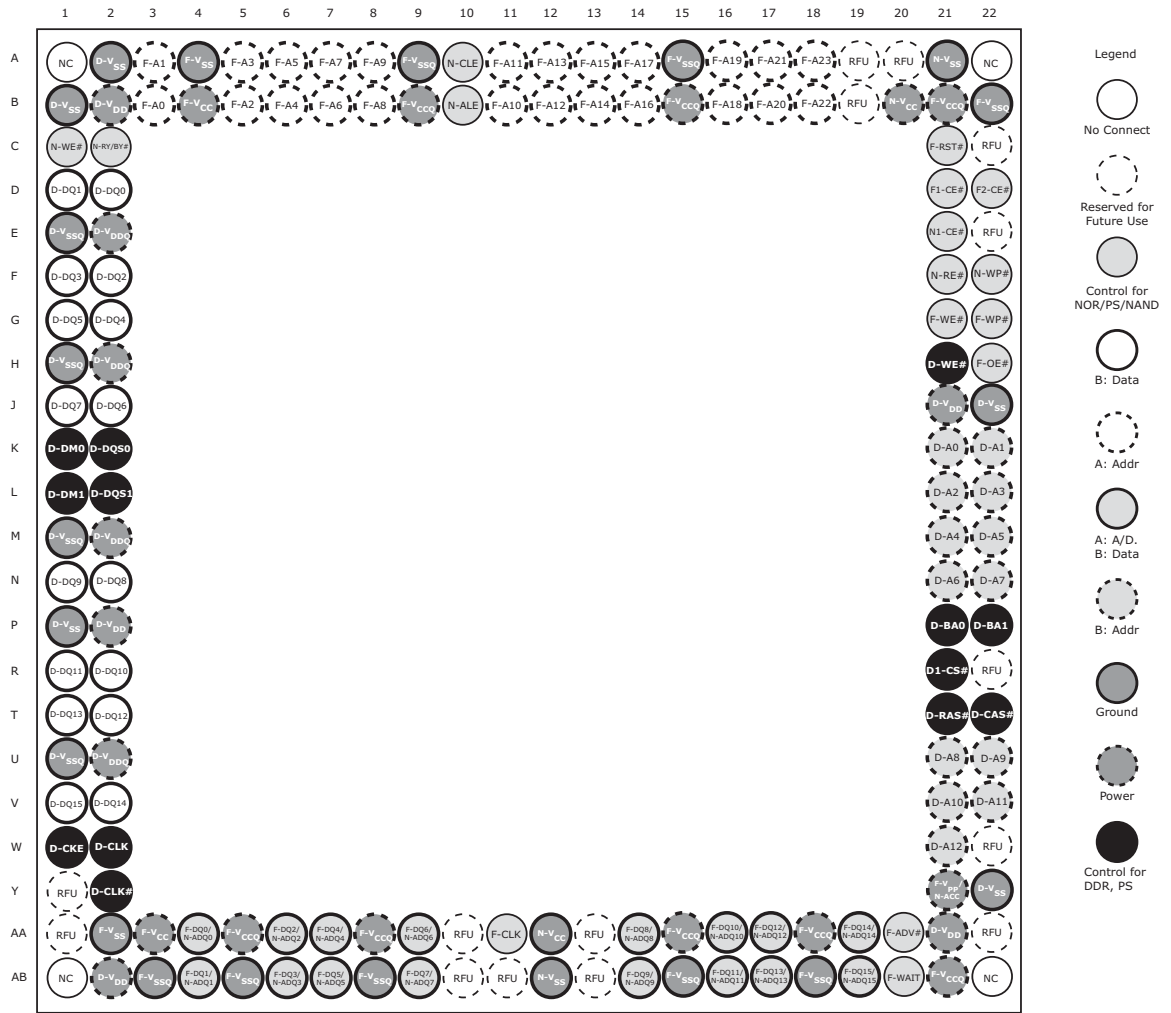


#### Special Handling Instructions For FBGA Package

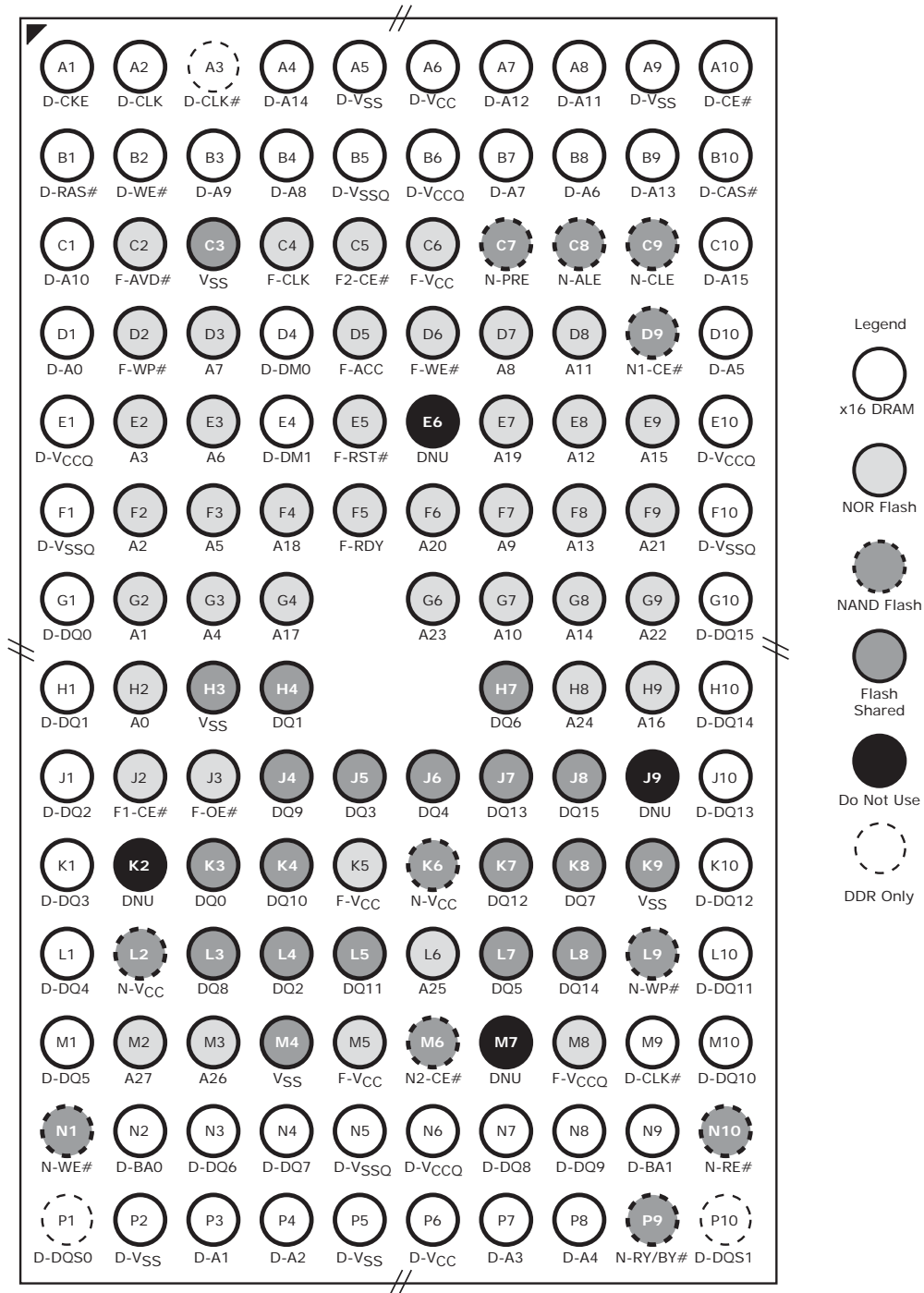
Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

### 3.6.2 Connection Diagram for 15 x 15 Package-on-Package



### 3.7 Lookahead Diagram on Split Bus



### 3.8 NOR Flash and DRAM Input/Output Descriptions

Signal	Description
A23-A0	NOR Flash Address inputs
DQ15-DQ0	Flash Data input/output, shared between NOR and ORNAND Flash. DQ0-DQ7 shared for x8 ORNAND
F2-CE#	NOR Flash Chip-enable input # 2. Asynchronous relative to CLK for burst mode.
F1-CE#	NOR Flash Chip-enable input #1. Asynchronous relative to CLK for Burst Mode.
OE#	NOR Flash Output Enable input. Asynchronous relative to CLK for Burst mode.
F-WE#	NOR Flash Write Enable input.
F-V <sub>CC</sub>	NOR Flash device power supply (1.7 V - 1.9 5 V).
F-V <sub>CCQ</sub>	Input/Output Buffer power supply.
V <sub>SS</sub>	Ground
RFU	Reserved for Future Use
RDY	Flash ready output. Indicates the status of the Burst read. V <sub>OL</sub> = data valid. Shared between NOR and ORNAND Flash.
CLK	NOR Flash Clock. The first rising edge of CLK in conjunction with AVD# low latches the address input and activates burst mode operation. After the initial word is output, subsequent rising edges of CLK increment the internal address counter. CLK should remain low during asynchronous access.
AVD#	NOR Flash Address Valid input. Indicates to device that the valid address is present on the address inputs. V <sub>IL</sub> = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V <sub>IH</sub> = device ignores address inputs
F-RST#	NOR Flash hardware reset input. V <sub>IL</sub> = device resets and returns to reading array data
F-WP#	NOR Flash hardware write protect input. V <sub>IL</sub> = disables program and erase functions in the four outermost sectors.
F-ACC	NOR Flash accelerated input. At V <sub>IH</sub> , accelerates programming; automatically places device in unlock bypass mode. At V <sub>IL</sub> , disables all program and erase functions. Should be at V <sub>IH</sub> for all other conditions.
D-A12-D-A0	SDRAM Address inputs
D-DQ15-D-DQ0	SDRAM Data input/output
D-CLK	SDRAM System Clock
D-CE#	SDRAM Chip Select
D-CKE	SDRAM Clock Enable
D-BA1-BA0	SDRAM Bank Select
D-RAS#	SDRAM Row Address Strobe
D-CAS#	SDRAM Column Address Strobe
D-DM1-D-DM0	SDRAM Data Input/Output Mask
D-WE#	SDRAM Write Enable input
D-VSS	SDRAM Ground
D-VSSQ	SDRAM Input/Output Buffer ground
D-VCCQ	SDRAM Input/Output Buffer power supply
D-VCC	SDRAM device power supply

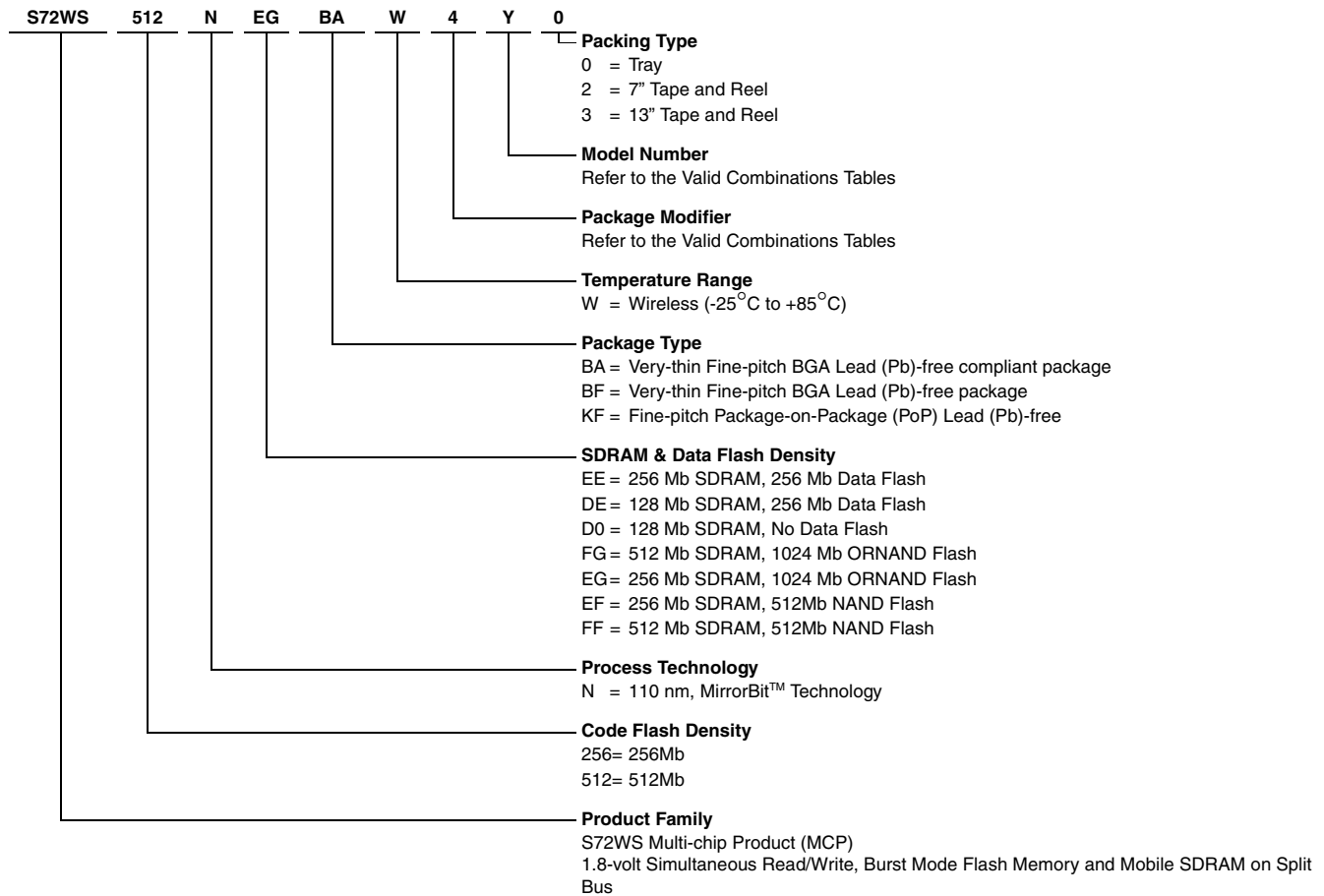
#### 3.8.1 ORNAND Signal Descriptions

Signal	Description
N-PRE	ORNAND Power-On Read Enable. Tie to V <sub>SS</sub> on customer board if not used
N-ALE	ORNAND Address Latch Enable
N-CLE	ORNAND Command Latch Enable
N-CE#	ORNAND Chip-enable
N-WP#	ORNAND Write-protect
N-WE#	ORNAND Write-enable
N-RE#	ORNAND Read-enable
N-RY/BY#	ORNAND Ready-Busy—this is shared with NOR RDY
N-I/O0-N-I/O15	ORNAND I/O Signals (I/O0-I/O7 for x8 bus width)
N-VCC	ORNAND Power Supply



## 4. Ordering Information

The order number is formed by a valid combinations of the following:



### 4.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

S72WS256ND0 Valid Combinations				NOR Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS256ND0	BFW	93	0, 2, 3 (Note 1)	66 MHz	Supplier 5	133 MHz	9x12x1.2mm 137-ball	(Note 2)I
	BAW, BFW	B7		54 MHz	Supplier 1	104 MHz		
		BB		66 MHz	Supplier 2	133 MHz	15x15x1.25mm 160-ball	
	KFW	D3			Supplier 5			

S72WS256NDE Valid Combinations				NOR Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS256NDE	BAW, BFW	U7	0, 2, 3 (Note 1)	54 MHz	Supplier 1	104 MHz	9x12x1.4mm 137-ball	(Note 2)
		UB			Supplier 2			

S72WS256NEE Valid Combinations				Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS256NEE	BAW, BFW	U7	0, 2, 3 (Note 1)	54 MHz	Supplier 1	104 MHz	9x12x1.4mm 137-ball	(Note 2)
		UB			Supplier 2			

S72WS512NFF Valid Combinations				Flash Speed	DRAM Supplier	DRAM Speed	Package	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS512NFF	BAW, BFW	ZJ	0, 2, 3 (Note 1)	66 MHz	DRAM Type 1	133 MHz	11 x 13 mm 137-ball	(Note 2)
	KFW						15 x 15 5mm 160-ball	
	BAW, BFW	Z2			DRAM Type 5		11 x 13 mm 137-ball	
	KFW						15 x 15 5mm 160-ball	
	BAW, BFW	ZT			DRAM Type 2		11 x 13 mm 137-ball	
	KFW						15 x 15 5mm 160-ball	

S72WS512NFG Valid Combinations				Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS512NFG	BAW, BFW	L7	0, 2, 3 (Note 1)	54 MHz	DRAM Type 4	104 MHz	11x13x1.4mm 137-ball	(Note 2)
		L6						
		L5						
		47						
		46						
		45						
		LZ			DRAM Type 2			
		LY						
		LW						
		4Z			DRAM Type 4			
		4Y						
		4W						
		N7						
		N6						
		N5						
		67			DRAM Type 2			
		66						
		65						
NZ								
NY								
NW								
6Z								
6Y								
6W								

S72WS512NEG Valid Combinations				Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS512NEG	BAW, BFW	LZ	0, 2, 3 (Note 1)	54 MHz	DRAM Type 2	104 MHz	11x13.1x1.4mm 137-ball	(Note 2)
		LY						
		LW						
		4Z						
		4Y						
		4W						
		NZ						
		NY						
		NW						
		6Z						
		6Y						
		6W						

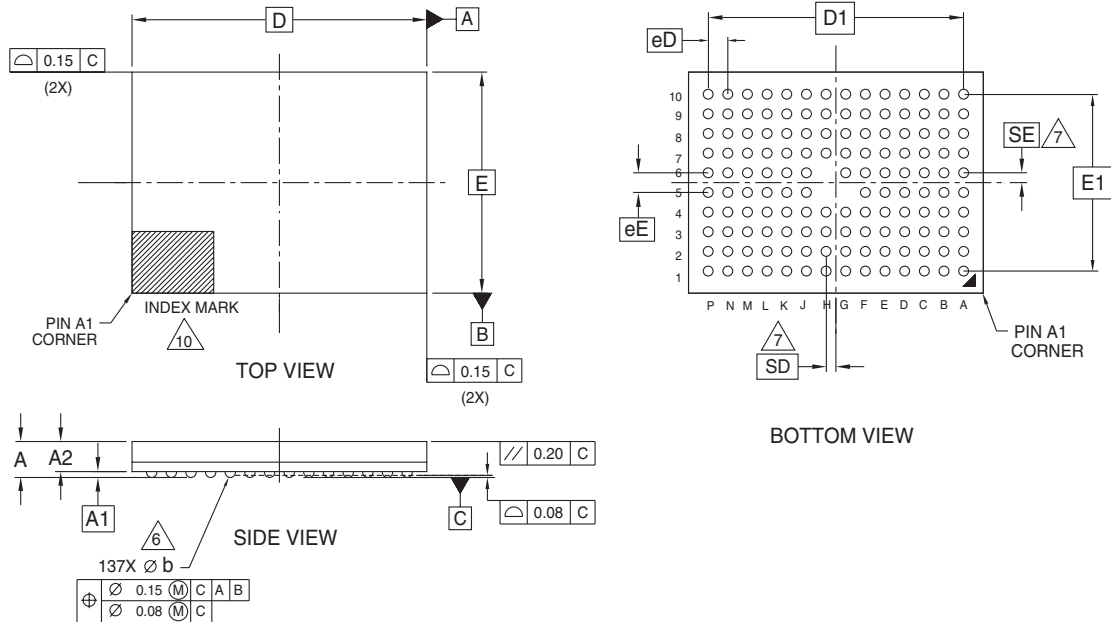
S72WS512NEF Valid Combinations				Flash Burst Speed	SDRAM Supplier	SDRAM Burst Speed	Package Type	Package Marking
Base Ordering Part Number	Package & Temperature	Model Number	Packing Type					
S72WS512NEF	KFW	HJ	0, 2, 3 (Note 1)	66 MHz	DRAM Type 2	133 MHz	15x15x1.2 mm 160-ball	(Note 2)

**Notes**

1. Packing Type 0 is standard. Specify other options as required.
2. BGA package marking omits leading "S" and packing type designator from ordering part number.

## 5. Physical Dimensions

### TLD137—137-ball Fine-Pitch Ball Grid Array (FBGA) 12 x 9 mm Package



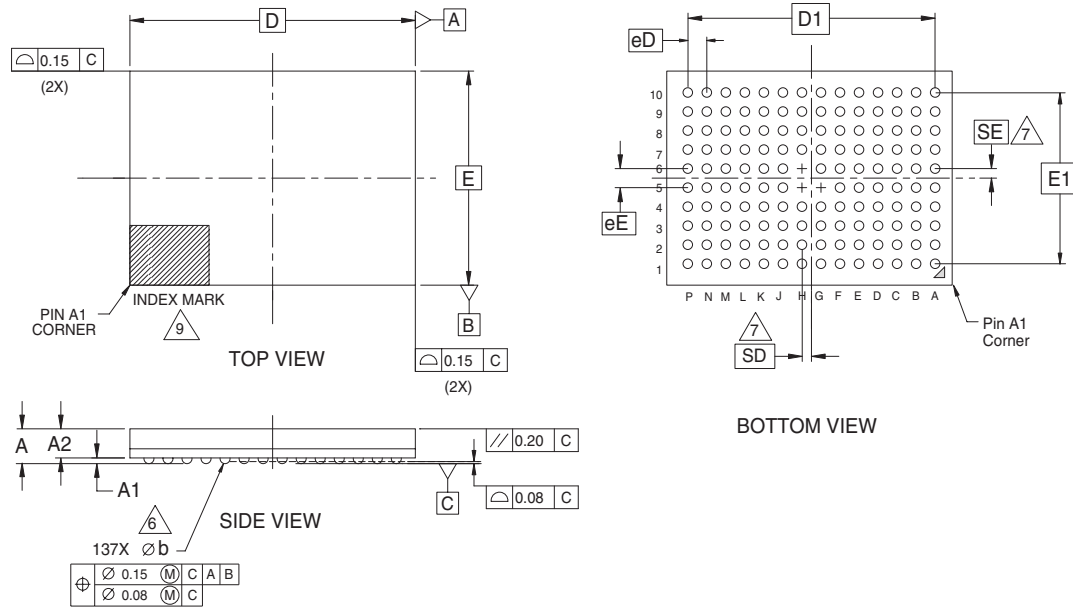
PACKAGE	TLD 137			
JEDEC	N/A			
D x E	12.00 mm x 9.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.20	PROFILE
A1	0.17	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	12.00 BSC.			BODY SIZE
E	9.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	137			BALL COUNT
$\phi$ b	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD / SE	0.40 BSC.			SOLDER BALL PLACEMENT
	G5,H5,H6			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
- $\square$  REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- $\triangle$  DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- $\triangle$  SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{e}{2}$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- N/A
- $\triangle$  A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3393; 16-038;22a

**FEA137—137-ball Fine-Pitch Ball Grid Array (FBGA) 13 x 11 mm Package**

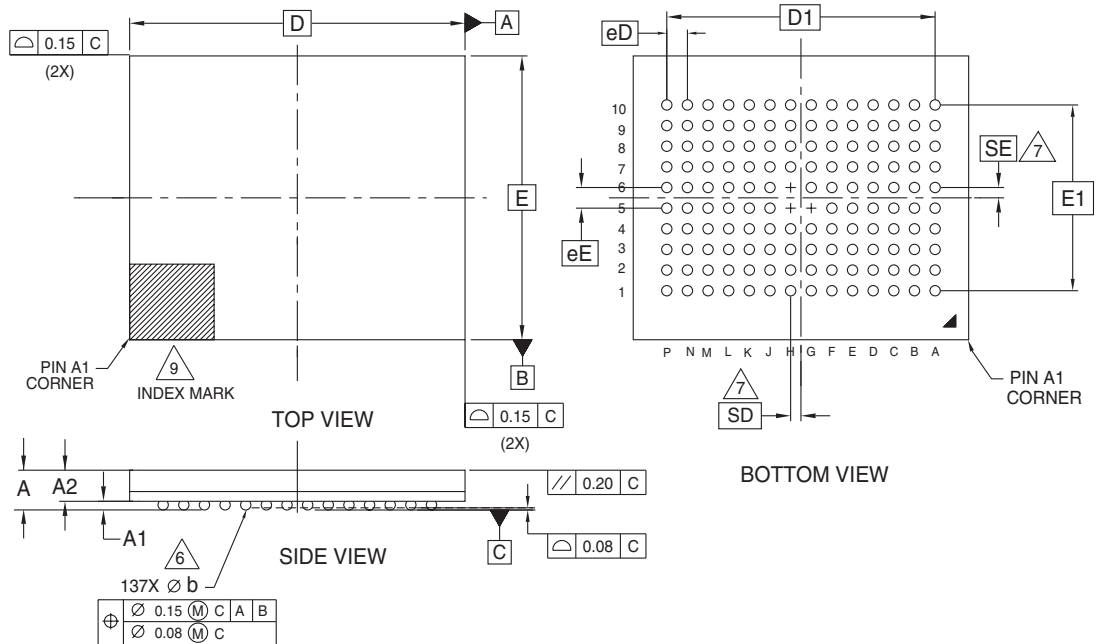


PACKAGE	FEA 137			NOTE
JEDEC	N/A			
D X E	12.00mm X 9.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	-	-	1.40	PROFILE
A1	0.10	-	-	BALL HEIGHT
A2	1.11	-	1.26	BODY THICKNESS
D	12.00 BSC			BODY SIZE
E	9.00 BSC			BODY SIZE
D1	10.40 BSC			MATRIX FOOTPRINT
	7.20 BSC			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	1.37			BALL COUNT
$\varnothing b$	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	G5, H5, H8			DEPOPULATED SOLDER BALLS

**NOTES:**

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

FVD137—137-ball Fine-Pitch Ball Grid Array (FBGA) 11 x 13 mm Package



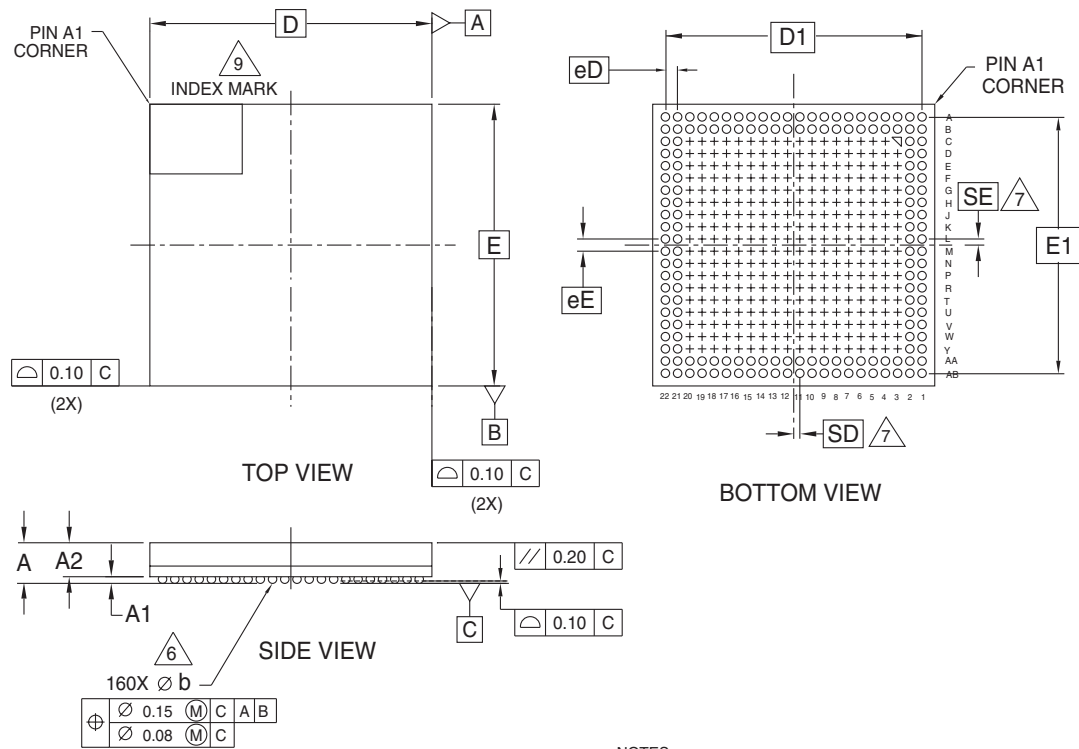
PACKAGE	FVD 137			NOTE
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.40	PROFILE
A1	0.10	---	---	BALL HEIGHT
A2	1.09	---	1.24	BODY THICKNESS
D	13.00 BSC.			BODY SIZE
E	11.00 BSC.			BODY SIZE
D1	10.40 BSC.			MATRIX FOOTPRINT
E1	7.20 BSC.			MATRIX FOOTPRINT
MD	14			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	137			BALL COUNT
Øb	0.35	0.40	0.45	BALL DIAMETER
eE	0.80 BSC.			BALL PITCH
eD	0.80 BSC.			BALL PITCH
SD SE	0.40 BSC.			SOLDER BALL PLACEMENT
	G5,H5,H6			DEPOPULATED SOLDER BALLS

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE =  $\frac{e}{2}$
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3522 \ 16-038.21 \ 09.29.05

**BWA160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package**



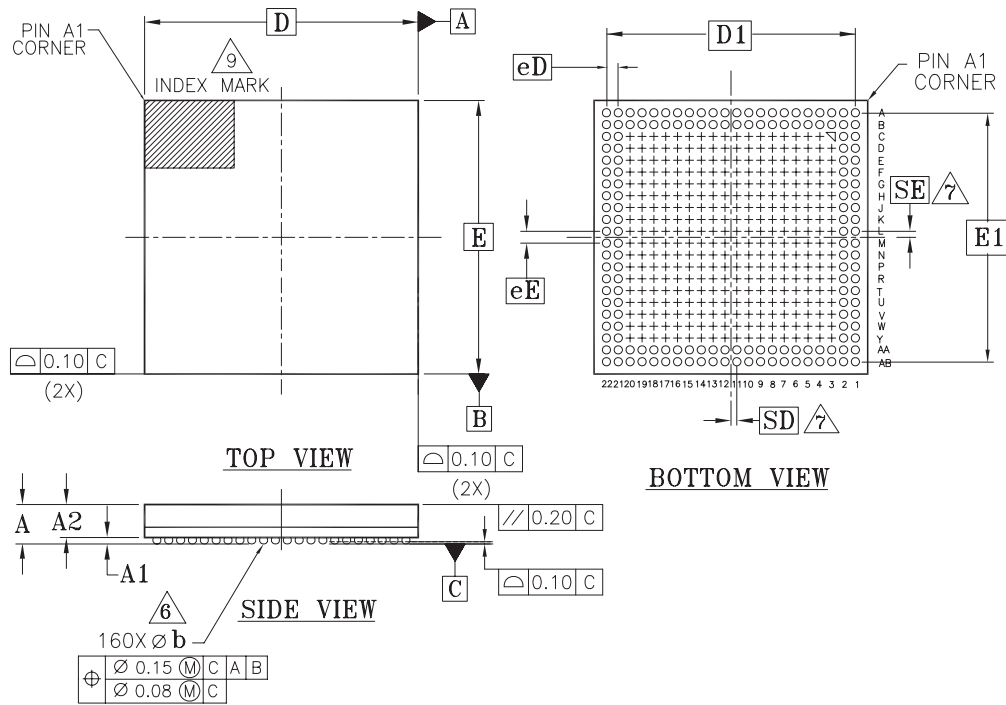
PACKAGE	BWA 160			NOTE
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.25	PROFILE
A1	0.35	---	---	BALL HEIGHT
A2	0.74	---	0.84	BODY THICKNESS
D	15.00 BSC.			BODY SIZE
E	15.00 BSC.			BODY SIZE
D1	13.65 BSC.			MATRIX FOOTPRINT
E1	13.65 BSC.			MATRIX FOOTPRINT
MD	22			MATRIX SIZE D DIRECTION
ME	22			MATRIX SIZE E DIRECTION
n	160			BALL COUNT
N	160			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PARAMETERS
$\varnothing b$	0.40	0.45	0.50	BALL DIAMETER
eE	0.65 BSC.			BALL PITCH
eD	0.65 BSC.			BALL PITCH
SD SE	0.325 BSC.			SOLDER BALL PLACEMENT
	C3-C20, D3-D20, E3-E20, F3-F20, G3-G20, H3-H20, J3-J20, K3-K20, L3-L20, M3-M20, N3-N20, P3-P20, R3-R20, T3-T20, U3-U20, V3-V20, W3-W20, Y3-Y20			DEPOPULATED SOLDER BALLS

**NOTES:**

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- [6] DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- [7] SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.  
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "-" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- [9] A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3518 \ 16-038.46 \ 02.23.06

**BWB160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package**



PACKAGE	BWB 160			NOTE
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.30	PROFILE
A1	0.38	---	---	BALL HEIGHT
A2	0.74	---	0.84	BODY THICKNESS
D	15.00 BSC.			BODY SIZE
E	15.00 BSC.			BODY SIZE
D1	13.65 BSC.			MATRIX FOOTPRINT
E1	13.65 BSC.			MATRIX FOOTPRINT
MD	22			MATRIX SIZE D DIRECTION
ME	22			MATRIX SIZE E DIRECTION
n	160			BALL COUNT
N	160			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PARAMETERS
Øb	0.43	0.48	0.53	BALL DIAMETER
eE	0.65 BSC.			BALL PITCH
eD	0.65 BSC.			BALL PITCH
SD / SE	0.325 BSC.			SOLDER BALL PLACEMENT
	C3 ~ C20, D3 ~ D20, E3 ~ E20, F3 ~ F20 G3 ~ G20, H3 ~ H20, J3 ~ J20, K3 ~ K20 L3 ~ L20, M3 ~ M20, N3 ~ N20, P3 ~ P20 R3 ~ R20, T3 ~ T20, U3 ~ U20, V3 ~ V20 W3 ~ W20, Y3 ~ Y20			DEPOPULATED SOLDER BALLS

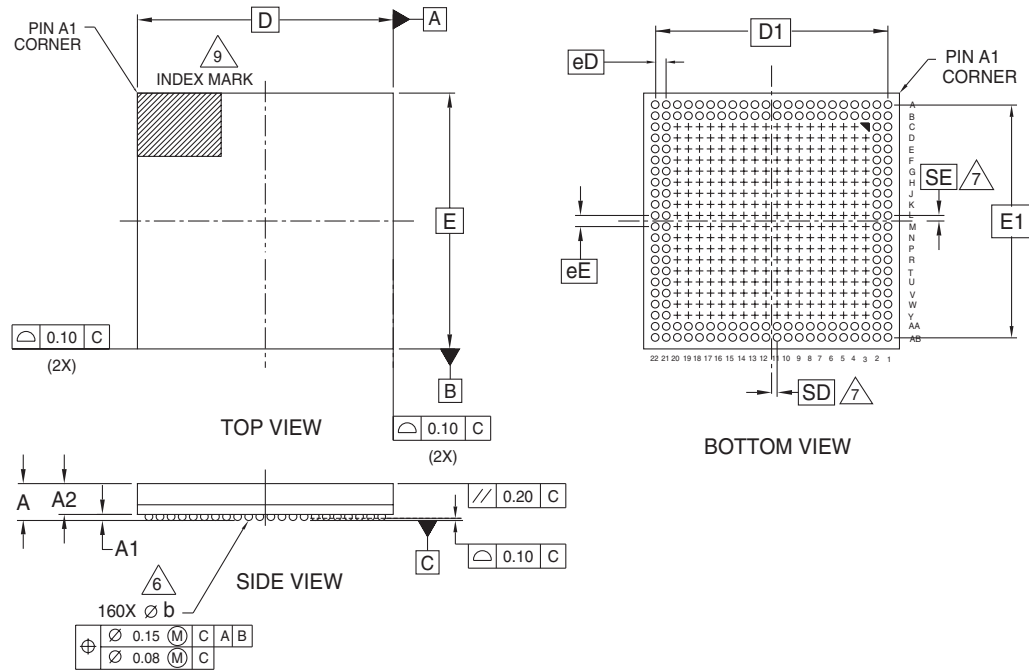
NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
- WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

3523.3 | 16-038.46 | 5.7.7



**BTA160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package**



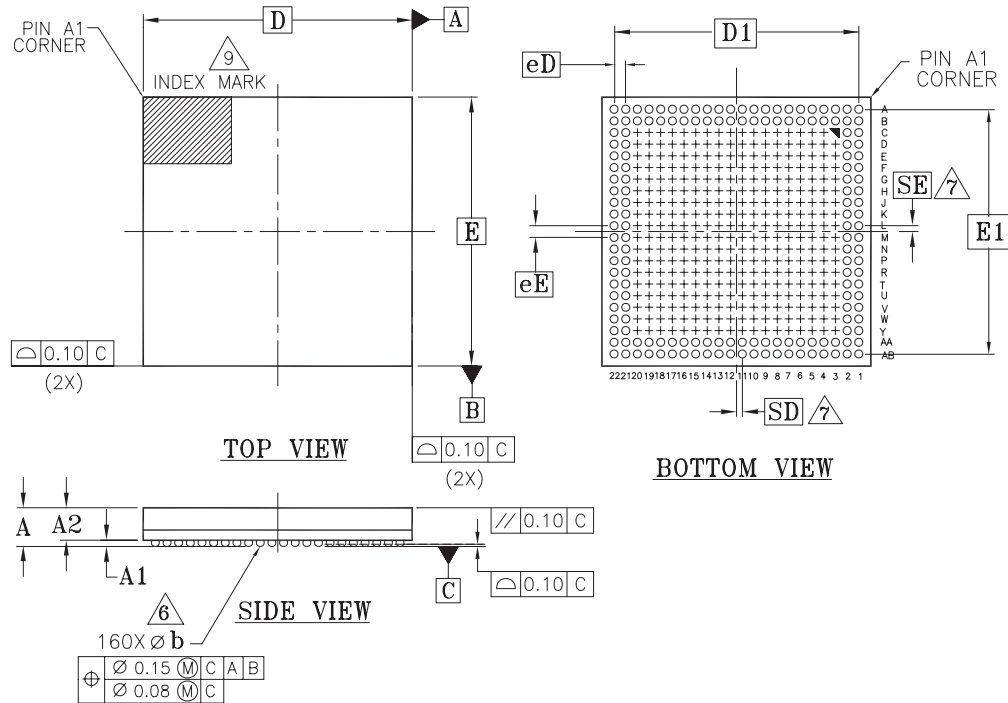
**NOTES:**

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.  
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
- WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.  
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
- OUTLINE AND DIMENSIONS PER CUSTOMER REQUIREMENT.

PACKAGE	BTA 160			NOTE
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	
A	---	---	1.30	PROFILE
A1	0.40	---	---	BALL HEIGHT
A2	0.74	---	0.84	BODY THICKNESS
[D]	15.00 BSC.			BODY SIZE
[E]	15.00 BSC.			BODY SIZE
[D1]	13.65 BSC.			MATRIX FOOTPRINT
[E1]	13.65 BSC.			MATRIX FOOTPRINT
MD	22			MATRIX SIZE D DIRECTION
ME	22			MATRIX SIZE E DIRECTION
n	160			BALL COUNT
N	160			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PARAMETERS
Ø b	0.45	0.50	0.55	BALL DIAMETER
[eE]	0.65 BSC.			BALL PITCH
[eD]	0.65 BSC.			BALL PITCH
[SD][SE]	0.325 BSC.			SOLDER BALL PLACEMENT
	C3-C20,D3-D20,E3-E20,F3-F20 G3-G20,H3-H20,J3-J20,K3-K20 L3-L20,M3-M20,N3-N20,P3-P20 R3-R20,T3-T20,U3-U20,V3-V20 W3-W20,Y3-Y20			DEPOPULATED SOLDER BALLS

3550 \ 16-038.55 \ 02.23.06

**ALH160—160-ball Fine-Pitch Ball Grid Array (FBGA) 15 x 15 mm Package**



PACKAGE	ALH 160			
JEDEC	N/A			
D x E	15.00 mm x 15.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.10	PROFILE
A1	0.38	---	---	BALL HEIGHT
A2	0.53	---	0.65	BODY THICKNESS
D	15.00 BSC.			BODY SIZE
E	15.00 BSC.			BODY SIZE
D1	13.65 BSC.			MATRIX FOOTPRINT
E1	13.65 BSC.			MATRIX FOOTPRINT
MD	22			MATRIX SIZE D DIRECTION
ME	22			MATRIX SIZE E DIRECTION
n	160			BALL COUNT
N	160			MAXIMUM NUMBER OF BALLS
R	2			NUMBER OF LAND PERIMETERS
Øb	0.43	0.48	0.53	BALL DIAMETER
eE	0.65 BSC.			BALL PITCH
eD	0.65 BSC.			BALL PITCH
SD   SE	0.325 BSC.			SOLDER BALL PLACEMENT
	C3 ~ C20, D3 ~ D20, E3 ~ E20, F3 ~ F20 G3 ~ G20, H3 ~ H20, I3 ~ I20, J3 ~ J20 K3 ~ K20, L3 ~ L20, M3 ~ M20, N3 ~ N20 P3 ~ P20, T3 ~ T20, U3 ~ U20, V3 ~ V20 W3 ~ W20, X3 ~ X20			DEPOPULATED SOLDER BALLS

**NOTES:**

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
- [e] REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.  
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

7 SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = [e/2]

- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

## 6. Revision History

Section	Description
<b>Revision A (August 26, 2004)</b>	
	Initial release
<b>Revision A 1 (June 1, 2005)</b>	
Global	Added SDRAM Type 2 module Added Lead (Pb)-free options Added FEA137 package diagram
<b>Revision A2 (October 7, 2005)</b>	
Global	Updated the S29WS-N NOR Flash Module Added the S30MS-P ORNAND Flash Module Added SDRAM Type 4 module
Product Selector Guide	Updated the Product Selector Guide
Connection Diagrams	Added two diagrams for the x8 and x16 ORNAND connections
Pin Descriptions	Updated descriptions and added descriptions for ORNAND signals
Ordering Information	Added new options Added Package-on-Package (PoP) options
Valid Combinations	Updated the valid combinations tables
Physical Dimensions	Added the FGA137 package diagram Added the BWA160 package diagram Added the BWB160 package diagram
<b>Revision A3 (November 9, 2005)</b>	
Global	Updated the SDRAM Type 1 module Changed the status of all RAM modules to Preliminary from Advanced.
<b>Revision A4 (December 14, 2005)</b>	
Product Selector Guide	Updated the tables
Connection Diagrams	Added the 512 Mb NOR Flash with 512 Mb NAND on Bus 1 and 512 Mb SDRAM on Bus 2 diagram
Ordering Information	Added new model number, package modifier and SDRAM & Data Flash density options
Valid Combinations	Updated all tables with new options
<b>Revision A5 (December 16, 2005)</b>	
Connection Diagrams	Updated the pinouts to include DDR signals Qualified 133 MHz as DDR based frequency
<b>Revision A6 (March 21, 2006)</b>	
NOR Flash + ORNAND Flash + DRAM MCPs Product Selector Guide	Updated the model numbers
Ordering Information	Updated the table
Valid Combinations	Updated the tables
Physical Dimensions	Added the ALH160 package
<b>Revision A7 (April 18, 2006)</b>	
Connection Diagrams	Updated the pinouts
<b>Revision A8 (June 1, 2006)</b>	
Global	Added 2 OPNs for products with DRAM Type 5 Updated product selector guide Updated valid combination table Added BTA160 package diagram
<b>Revision A9 (May 8, 2007)</b>	
Physical Dimensions	Added the ALH 160 package diagram

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